CLAIMS

What is claimed is:

1. A memory system for a computer, the memory system comprising a single memory page including a kernel stack and a register stack engine (RSE) stack.

2. The memory system of claim 1, wherein the kernel stack and the RSE stack grow in opposite directions.

3. The memory system of claim 2, wherein the single memory page further includes a "uarea" data structure.

4. The memory system of claim 3, wherein the uarea data structure is located between the kernel stack and the RSE stack.

5. The memory system of claim 2, further comprising:
a first red zone in a second memory page bordering a first memory region of the single memory page which is allocated to the kernel stack.

6. The memory system of claim 5, further comprising:
a second red zone in a third memory page bordering a second memory region of the single memory page which is allocated to the RSE stack.

7. The memory system of claim 3, wherein a number of translation lookaside buffer (TLB) misses when a process "enters" a kernel of an operating system of the computer is no more than one TLB miss.

8. The memory system of claim 2, wherein the memory system further comprises a stack overflow handler that is configured to allocate more memory to one of the stacks if it overflows.

9. The memory system of claim 1, wherein the memory system is used in cooperation with an operating system for the computer, and wherein the operating system comprises a flavor of UNIX.

10. The memory system of claim 1, wherein the memory system is used in cooperation with at least one microprocessor with an IPF processor architecture.

11. A computer system comprising:
a microprocessor including a register stack and a register stack engine (RSE);
an operating system including a kernel; and
a memory system configured to have a single memory page that includes both a kernel stack and an RSE stack.

12. The computer system of claim 11, wherein the kernel stack and the RSE stack grow in opposite directions.

13. The computer system of claim 12, wherein the single memory page further includes a "uarea" data structure.

14. The computer system of claim 13, wherein the uarea data structure is located between the kernel stack and the RSE stack in the memory system.

15. The computer system of claim 12, further comprising:
a first red zone in a second memory page bordering a first memory region of the single memory page which is allocated to the kernel stack.

16. The computer system of claim 15, further comprising:
a second red zone in a third memory page bordering a second memory region of the single memory page which is allocated to the RSE stack.

17. The computer system of claim 13, wherein a number of translation lookaside buffer (TLB) misses when a process "enters" a kernel of the operating system is no more than one TLB miss.

18. The computer system of claim 12, wherein the memory system further comprises a stack overflow handler that is configured to allocate more memory to one of the stacks if it overflows.

19. The computer system of claim 11, wherein the microprocessor is configured with an IPF processor architecture.

20. The computer system of claim 11, wherein the operating system comprises a flavor of UNIX.

21. A method of a process entering a kernel of an operating system configured for an IPF processor architecture, the method comprising:
accessing a kernel stack within a memory page;
accessing an RSE stack within the same memory page; and
accessing a uarea data structure within the same memory page.